ATARI FALCON030

Technical Documentation

October 1st, 1992

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SECTION ONE
INTRODUCTION

1.0 OVERVIEW

The latest enhancement to the Atari® ST™ architecture is the Atari FALCON030™ system. The system is comprised of an integrated housing which contains the CPU, System RAM, Floppy Disk, Optional Hard Disk, modular keyboard, and Power supply. A detachable mouse is also included. The system is compatible with previous designs including the STE™, and MEGA STE™.

The basic system is shipped with 1, 4, or 14 Mbytes of RAM, 512 Kbytes of ROM, 2 Mbyte (unformatted) Floppy Disk Drive, and high speed Motorola® MC68030FG™ CPU running at 16 MHz. FALCON030 also offers system expansion via an internal expansion connector.

1.1 SYSTEM FEATURES

Basic system features contained in the FALCON030 are as follows:

- MC68030FG Microprocessor running at 16 MHz
- Optional MC68881/MC68882 Coprocessor running at 16 MHz
- 1, 4, or 14 MB RAM
- 512 KB ROM
- Graphics Coprocessor (Blitter)
- ST™, VGA, True Color, and Programmable Video Modes
- Digital stereo sound
- Digital Signal Processor
- Parallel Port
- One RS232 Port
- MIDI Interface
- Cartridge Port
- External SCSI II DMA Port
- STE Compatible Joystick ports
- LAN Port
- 3½" 2 Mbyte Floppy Drive (unformatted)
- Internal Optional IDE Hard Disk
- 100 DPI Mouse
- Real-Time Clock
- Expansion Port

1.2 CASE DESIGN

1.2.1 FRONT VIEW

The front of the FALCON030 system includes LEDs for power, floppy disk access, and if an optional hard disk is installed, hard disk access. See Figure 1.

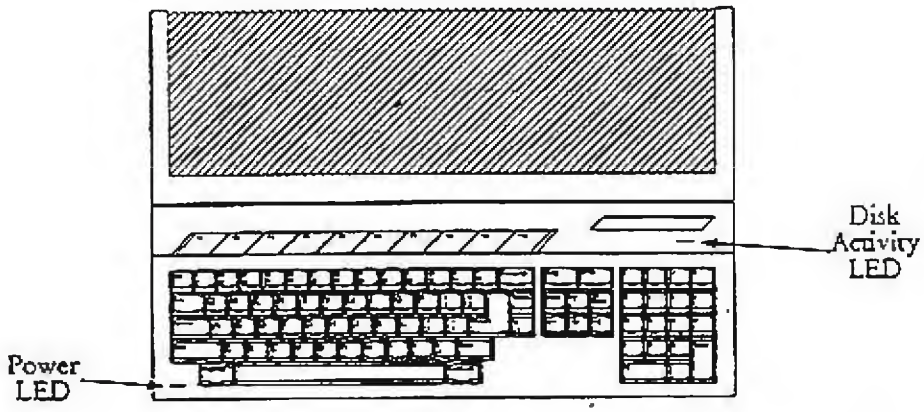


Figure 1

1.2.2 REAR VIEW

The rear of the FALCON030 system contains connectors for the digital audio interface, stereo jacks, SCSI II connector, monitor out/genlock, RF out, parallel port, serial port, LAN, reset button, on/off switch, and AC input. See Figure 2.

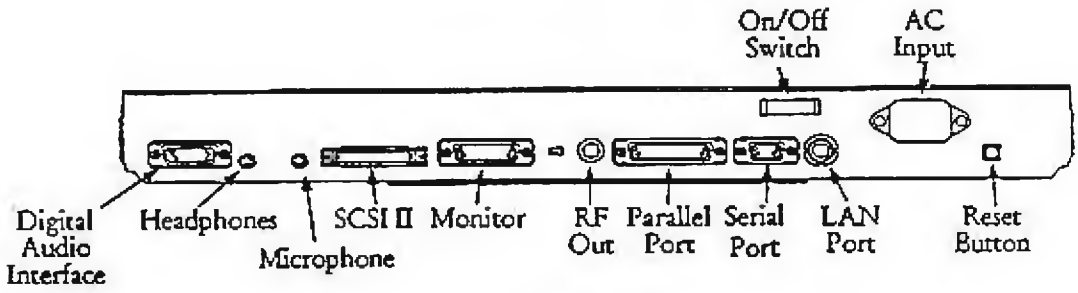


Figure 2

1.2.3 LEFT SIDE VIEW

The left side of the FALCON030 contains the cartridge port and game ports A and B. See Figure 3.

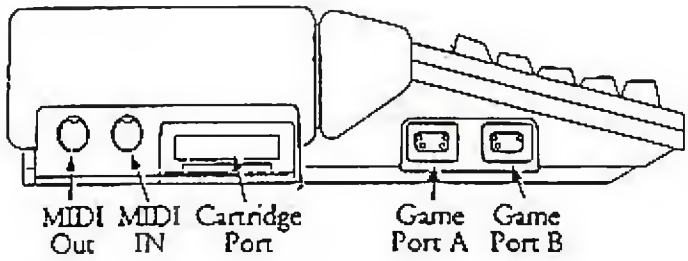


Figure 3

1.2.4 RIGHT SIDE VIEW

The right side of the FALCON030 contains the Floppy Disk Drive. See Figure 4.

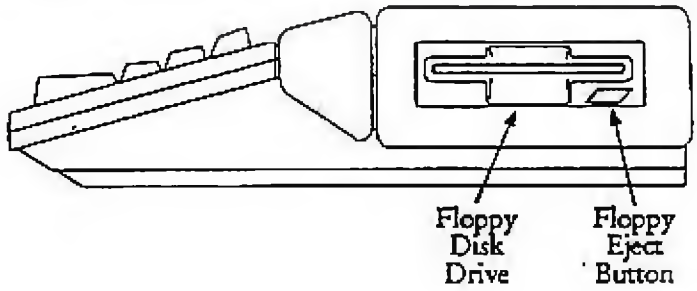


Figure 4

1.2.5 Bottom View

The bottom of the FALCON030 contains the Mouse/Joystick and Joystick connectors. See Figure 5.

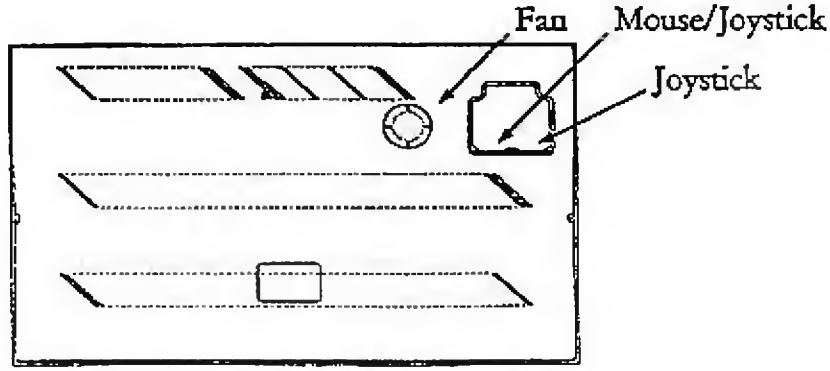


Figure 5

1.3 POWER SUPPLY

The system includes a switching power supply which is configured for 110 volt AC input US or 220/240 volt AC input European. The power supply provides 37.4 watts of power to the system. Voltages of +12V and +5V are provided to the main logic board as well as voltages for the floppy drive and optional hard disk.

1.3.1 SPECIFICATIONS

1.3.1.1 AC Input

Input	Country	
	U.S.	Europe
Voltage:	90 to 129 VAC (RMS) 117 VAC Nominal	198 to 264 VAC (RMS) 230 VAC Nominal
Frequency:	55 to 65 Hz	45 to 55 Hz
Current:	0.9 Amperes (RMS)	0.45 Amperes (RMS)
Maximum Inrush Current:	35 Amperes	35 Amperes

1.3.1.2 DC Output

Output	Voltage	
Voltage:	+5 VDC	+12 VDC
Minimum Load Current:	1.5 Amp	0.0 Amp
Maximum Load Current:	7.0 Amp	0.2 Amp
Line Regulation:	5%	10%
Load Regulation:	5%	10%
Cross Regulation:	5%	10%
Ripple:	100 millivolts p-p	100 millivolts p-p
Noise:	100 millivolts p-p	100 millivolts p-p

1.3.1.3 Operational Characteristics

Output	Characteristic
Peak Current:	+5 VDC peak current of 10 amperes for not more than 10 seconds with +12 VDC output at full load.
+5 VDC Set Point:	The +5 VDC output must be set to +5.05 0.1 VDC with a +5 VDC output having a load of 4.0 amperes.
Total Output Power:	37.4 watts
Efficiency:	55% minimum at full load, minimum frequency.
Hold Up Time:	10 milliseconds at 100% load and nominal input voltage.
Switching Frequency:	20 KHZ (minimum)
Temperature Coefficient:	0.04% per degree Centigrade
Power On Delay Time:	150 milliseconds (maximum)
Short Circuit Protection:	The power supply should switch off within 20 milliseconds
Overshoot:	(5% of the nominal output voltage) at turn on and off with the outputs not exceeding the limit.
Operating Temperature:	0 to +50 degrees Centigrade
Operating Humidity:	20% to 90% Relative Humidity
Operating Altitude:	0 to 3000 meters

SECTION TWO
THEORY OF OPERATION

2.0 OVERVIEW

The section discusses in general the components which make up the FALCON030 system and how they interrelate with one another. This will give you a basic working knowledge of the system's architecture necessary to repair most hardware failures which may occur. Other sections are provided in this manual to aid in use of diagnostics and troubleshooting techniques. The system is divided into three main categories. Main system, Audio/Video Subsystem, and I/O Subsystem. Each category will be covered separately along with any other components that may lie outside that section as it relates to that section's function within the system.

2.1 MAIN SYSTEM

The components which make up the main system are as follows:

- Motorola MC68030FG Microprocessor
- Optional Motorola MC68881/MC68882 Coprocessor
- 512 Kbyte ROM
- 1, 4, 14 Mbytes RAM
- COMBO IC
  - Memory Control Unit (MCU)
  - Clock Dividers
  - Interrupt Priority and Illegal Condition Detection
  - Chip Selects
  - Paddle Circuitry
  - Joystick Circuitry
  - Light Gun Circuitry
  - BLITTER
- DMA Support (SDMA IC)
- Real-Time Clock (1287 IC)
- System Timing and Bus Control (SDMA)
- Configuration Switch (S56, S57)

2.1.1 MC68030 Microprocessor

The Motorola MC68030FG is a 32-bit enhanced microprocessor which contains a central processing unit (CPU), enhanced bus controller, 256 byte instruction and data caches, and a memory management unit (MMU). The microprocessor is operated at 16 MHz.

The MC68030FG implements sixteen 32-bit general purpose data registers, two 32-bit supervisor stack pointers, ten special purpose control registers, and separate 32-bit non multiplexed address and data bus.

2.1.1.1 MC68030FG Pin List and Signal Description

General Function			
Pin	Signal	Type	Description
12,10,9	FC0-FC2	Output	3-bit function code used to identify the address space of each bus cycle.
21-22,58-58,33-31,29-26,36,24-23,56-51,48	A0-A31	Output	32-bit address bus.
75-76,78-83,86-89,91-94,96-99,101-104,106-109,11-114	D0-D31	I/O	32-bit data bus.
120,119	SIZ0-SIZ1	Output	Transfer Size bits indicate the number of bytes remaining to be transferred for the current bus cycle. These signals together with A0 and A1 define the active sections of the data bus.
Bus Control Signals			
Pin	Signal	Type	Description
117	R/(W)-	Output	Read/Write- indicates whether the current bus cycle is a read or write cycle. When low it indicates a write cycle, when high it indicates a read cycle.
124	DS-	Output	Data Strobe indicates that a device should put valid data on the data bus during a read cycle. During a write cycle this signal indicates that the MC68030 has placed valid data on the bus.
125	AS-	Output	Address Strobe indicates that a valid address is on the adress bus. The R/(W)-, FC0-FC2, and SIZ0-SIZ1 are also valid when this signal is asserted.
3,132	DSACK0 DSACK1	Input	Data Transfer and Size Acknowledge 0 and 1 indicate the completion of a requested data transfer operation and also indicate the size of the external bus port at the end of that completion.

Bus Control Signals			
Pin	Signal	Type	Description
131	STERM-	Input	Synchronous Termination indicates that the addressed port size is 32-bits and that the data is to be latched on the next falling clock edge for a read cycle. This active lowsignal is tied high in the FALCON030 System.
Cache Control Signals			
Pin	Signal	Type	Description
122	CIIN-	Input	Cache Inhibit Input prevents data from being loaded into the MC68030 instruction and data caches. This signal is ignored during all write cycles.
Interrupt Control Signals			
Pin	Signal	Type	Description
70,69,68	IPL0- IPL1- IPL2-	Input	Interrupt Priority Level 0-2 provide an indication of an interrupt condition and the encoding of the interrupt level from a peripheral or external prioritizing logic. IPL2- is the most significant bit of the level number.
7	AVEC-	Input	Autovector indicates that the MC68030 should generate an automatic vector during an interrupt acknowledge cycle.
Bus Control Signals			
Pin	Signal	Type	Description
20	BR-	Input	Bus Request indicates that an external device needs to become the bus master.
16	BG-	Output	Bus Grant indicates that the MC68030 will release ownership of the bus when the current processor bus cycle completes.
17	BGACK-	Input	Bus Grant Acknowledge indicates that an external device has become bus master.
Bus Exception Control Signals			
Pin	Signal	Type	Description
84	RESET-	I/O	Reset is used to initiate a system reset. As an input the MC68030 is reset. As an output only external devices are reset.
129	HALT-	Input	Halt indicates that the processor should suspend bus activity or, when used with BERR, that the processor should retry the current cycle.
130	BERR-	Input	Bus Error indicates that an invalid bus operation is being attempted or, when used with HALT-, that the processor should retry the current bus cycle.

Other Signals			
Pin	Signal	Type	Description
6	CLK	Input	Clock is the input clock to the MC68030. In the FALCON030 system it can be selected through the COMBO IC to be either 16 MHz or 8 MHz.
65,71,73	EM0 EM1 EM2	Input	Emulator support signals. These signals are tied high.
L6, K4, K10, H3, H11, F2, F11, D4, D10, C6	Vcc	Input	Power supply for MC68030
L5, L7-L9, J3, J11, G3, G11, F3, F11, E3, E11, C5, C7, C9	GND	Input	Ground for MC68030.

2.1.2 Optional MC68882 Coprocessor

The FALCON030 system comes equipped with a socket for an optional Motorola MC68881/MC68882 coprocessor. The coprocessor interfaces to the MC68030 via standard MC68000 bus transfers and is clocked at the same rate as the MC68030. Both data transfers and exception processing are done at the request of the coprocessor, allowing memory management, address errors, bus errors, and bus arbitration to function as if the instructions were being executed by the MC68030.

2.1.2.1 MC68882 Pin List and Signal Description

Pin	Signal	Type	Description
26-22	A0-A4	Input	Address Bus signals are used by the MC68030 to select the CIR locations in the CPU address space. Both.A0 and SIZE- signals are tied high in the FALCON030 system to indicate a 32-bit data bus.
1,2,3,64-68,62,60-33	D0-D31	I/O	Data Bus signals D0-D31 serve as the general-purpose data path between the MC68030 and MC68882.

Pin	Signal	Type	Description
18	SIZE-	Input	Size is used in conjunction with the A0 signal to configure the MC68882 for 32-bit operation. SIZE- is tied high in the FALCON030 system for 32-bit data bus operation.
21	AS-	Input	Address Strobe indicates a valid address on the address bus and valid signals for chip select (CS-) and Read/Write (R/(W)-).
29	CS-	Input	Chip Select enables the MC68030 to access the MC68882's CIRs.
28	R/(W)-	Input	Read Write indicates the direction of a bus transaction. A high indicates a read from the MC68882, a low indicates a write to the MC68882.
20	DS-	Input	Data Strobe indicates that valid data is on the data bus during a write bus cycle.
31-32	DSACK0- DSACK1-	Output	Data Transfer Size and Acknowledge 0 and 1 indicate the completion of a bus cycle to the MC68030. The MC68882 asserts both signals upon the assertion of CS-.
13	RESET-	Input	Reset causes a reset of the MC68882.
11	CLK	Input	Clock is the input clock of the MC68882 and is the same frequency as the input clock of the MC68030.
4	SENSE-	I/O	Sense is tied high in the FALCON030 system to indicate the MC68882 is present.
10,16,17, 27,43,52-53, 61	Vcc	Input	Power for the MC68882.
5,6,7,8,9, 12,14,19, 30,41,51, 63	GND	Input	Ground for the MC68882.

2.1.3 ROM

One socket is provided in the system for the installation of ROM (read only memory) IC. The total amount of ROM shipped with the system is 512Kbytes. The ROM is accessed through an 18-bit bus path via the ADDR1-ADDR18 lines.

The system ROM also provides an 16-bit data path via the DATA0-DATA15 lines. By default the system supports 125ns ROMs. An image of the first eight bytes of ROM resides in the first eight bytes of the system RAM area. The first eight bytes, located at 0x00000000-0x00000007, are accessible only in supervisor mode.

Any attempt to write or attempt to read from this in user mode causes a bus error. The full ROM memory map resides at addresses 0x00E00000-0x00EFFFFF.

The tasks performed by the system ROM are as follows:

- System Initialization
- Boot from Floppy or Hard disk
- TOS Operating System

2.1.4 System RAM

System RAM is physically made up of a daughter card containing 8 256K X 4, 8 1M X 4, or 32 4M X 1 DRAMs located in two banks. This architecture yields configurations of 1 Mbyte, 4 Mbytes, or 16 Mbytes of RAM used in a dual-purpose role for both system memory and video memory.

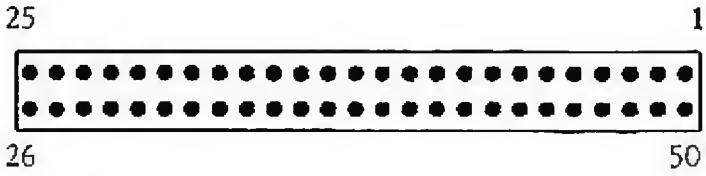
The daughter board is plugged into the main logic card via a 30-pin and 50-pin dual connector. This implementation also provides a full 32-bit data path to the VIDEL IC via the D0-D31 data bus lines. The standard configuration shipped with the system is 1Mbyte. Even though a total of 16 Mbytes of RAM may be available with 4M X 1 DRAMs installed, for compatibility with the STE, only 14 Mbytes of RAM may be accessed.

The RAM is addressed via eleven address lines (A0-A10). Row and Column selection is accomplished through the XRAS0, XRAS1, XCAS0L, XCAS0H, XCAS1L, and XCAS1H signals. Write enable for the RAM is provided by the XWE signal. On-board accesses to RAM are usually four clock cycles long, with no parity or ECC correction. Video data is accessed using fast page mode in bursts of 17 32-bit words. The data will fill the video FIFO in the VIDEL IC. The Memory Daughter Board identifies the amount of RAM present via two pins used on the Memory Daughter Board 50-pin connector.

The first 800 bytes, 0-0x800, are accessible only in supervisor mode. Any attempt to read or write to these locations in user mode causes a bus error.

2.1.4.1 System RAM Connector Pin List

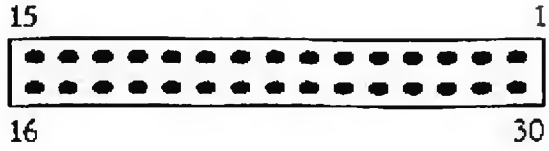
2.1.4.1.1 50-in Connector J17



50-Pin Connector J17

Pin	Signal	Pin	Signal
1	Ground	2	Vcc
3	Memory Data 15	4	Memory Data 14
5	Memory Data 13	6	Memory Data 12
7	Memory Data 11	8	Memory Data 10
9	Ground	10	Vcc
11	Memory Data 9	12	Memory Data 8
13	Memory Data 7	14	Memory Data 6
15	Memory Data 5	16	Ground
17	Vcc	18	Memory Data 4
19	Memory Data 3	20	Memory Data 2
21	Memory Data 1	22	Memory Data 0
23	Memory Size 0	24	Ground
25	Vcc	26	Ground
27	Vcc	28	Memory Data 16
29	Memory Data 17	30	Memory Data 18
31	Memory Data 19	32	Memory Data 20
33	Memory Data 21	34	Ground
35	Vcc	36	Memory Data 22
37	Memory Data 23	38	Memory Data 24
39	Memory Data 25	40	Memory Data 26
41	Ground	42	Vcc
43	Memory Data 27	44	Memory Data 28
45	Memory Data 29	46	Memory Data 30
47	Memory Data 31	48	Memory Size 1
49	Ground	50	Vcc

2.1.4.1.2 30-Pin Connector J6



30-Pin Connector J6

Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	Ground	4	Memory Address 8
5	Memory Address 7	6	Memory Address 6
7	Memory Address 5	8	Memory Address 4
9	Memory Address 3	10	Memory Address 2
11	Memory Address 1	12	Memory Address 0
13	Ground	14	Vcc
15	Vcc	16	Ground
17	Ground	18	Vcc
19	Memory Address 10	20	Memory Address 9
21	Write Enable	22	Row Address Select 0
23	Row Address Select 1	24	Column Address Select 0 High
25	Column Address Select 0 Low	26	Column Address Select 1 High
27	Column Address Select 1 Low	28	Ground
29	Vcc	30	Vcc

2.1.5 COMBO IC

The COMBO IC contained in the FALCON030 system integrates several functions. These can be summarized as follows:

- Memory Control Unit (MCU)
- Interrupt Priority and Illegal Condition Detection
- Clock Dividers
- Chip Selects
- Paddle Circuitry
- Joystick Circuitry
- Light Gun Circuitry
- Blitter (Graphics Coprocessor)

2.1.5.1 Memory Control Unit (MCU)

The Memory Controller portion of the COMBO IC takes addresses from the address bus (A1-A23) and converts them to Row and Column Addresses for DRAM with RAS and CAS Strobes. It also generates chip selects for ROM and I/O peripherals. All RAM accesses are controlled by the MCU, which is programmable for up to 14 Megabytes of memory.

Memory size is determined via two configuration pins set in hardware on the Memory Daughter Board. The Memory Controller refreshes the dynamic RAMs and loads the VIDEL IC with display data. The Memory Controller produces all of the addresses for video, refresh, and CPU/DMA on the multiplexed address bus.

2.1.5.2 Interrupt Mask and Status Control

The COMBO IC in the FALCON030 system is used both for the masking of interrupts and the storing of current interrupt status. The interrupt priorities in the system are as follows:

Interrupt Level	Priority
7 (Highest)	Open (Bus)
6	MFP Interrupts and DSP
5	85C30 LAN IC
4	Vertical Blanking (VSYNC)
3	Open (Bus)
2	Horizontal Blanking (HSYNC)
1 (Lowest)	Open (Bus)

Hardware within the COMBO IC allows the enabling of interrupt levels 1 and 3 as external VPA positive edge interrupts. This allows the use of either interrupt level for devices such as the parallel port or IDE port. Hardware is also present allowing the use of interrupt level 5 as a external negative edge interrupt. The COMBO IC uses the output signals IPL0-IPL2 to tell the microprocessor the priority of the interrupt being requested.

2.1.5.2.1 Interrupt Priority Level Signal Definition

IPL2	IPL1	IPL0	Interrupt Level
1	1	0	Level 1
1	0	1	Level 2
1	0	0	Level 3
0	1	1	Level 4
0	1	0	Level 5
0	0	1	Level 6
0	0	0	Level 7

2.1.5.3 Bus Error Circuitry and Illegal Condition Detect

Bus error circuitry is contained in the COMBO IC that causes a bus error signal (BERR) to be sent to the 68030 if certain conditions occur. These conditions are listed as follows:

- A bus cycle is not concluded within 16 micro seconds (programmable to 32usec)
- An attempt to write to ROM
- Writing the wrong size data into a register
- Writing system memory when in user mode

2.1.5.4 Clock Dividers

The COMBO IC takes the 32-MHz clock and outputs 16 MHz, 8 MHz, 4 MHz, and 500-kHz clocks.

2.1.5.5 Chip Selects

The COMBO IC decodes addresses to generate chip selects to the 6850s (N6850), MFP (MFPSC), VIDEL Video Chip (VCS), Real-Time Clock (RTCCS), Programmable Sound Generator (SNDCS), Coprocessor (FPUCS), Memory Controller, Cartridge ROM (ROM3, ROM4), IDE Hard Disk (HIDECS0, HIDECS1), and Operating System ROM (ROM2).

2.1.5.6 Paddle Circuitry

The COMBO IC contains the circuitry necessary to interface a pair of paddles through the joystick port. Input signals PAD0X, PAD1X, PAD0Y, and PAD1Y are used for direction control feed from the paddles themselves. The PADRST signal is used as a paddle reset.

2.1.5.7 Joystick Circuitry

The COMBO IC also contains the circuitry necessary to support the interface of a pair of joysticks to the system. Input signals JOYRH and JOYRL are read enables, while JOYWH and JOTWL are write enables. The BUTTON signal is used as a fire button enable signal.

2.1.5.8 BLITTER

The BLITTER contained inside the COMBO IC is a graphics coprocessor designed to handle the extra burden of graphics video generation on the microprocessor. This section performs bit aligned block transfers required in graphics generation, which adds to the capabilities of the microprocessor. The BLITTER section also contains a barrel shifter.

2.1.5.9 Light Gun Circuitry

The light gun causes a pulse on the XPEN signal which is used in the COMBO IC to latch the current values of the horizontal and vertical counters. This value can then be read by the microprocessor to determine the raster position of the light gun.

2.1.5.10 COMBO IC Pin List and Signal Description

Pin	Signal	Type	Description
1	BMODE	Input	The BMODE pin is used to indicate to the COMBEL IC whether the current bus master is a 68030 or 68000 type device. When a 68030 type device is the bus master the BMODE pin will be pulled low. The BMODE pin is normally pulled high, indicating 68000 type bus masters.
95,90,82, 68,65,63, 29,24,17, 15,12,7, 188,185, 178,177, 170,162, 143,135, 128,126, 121	A1-A23	I/O	This 23 bit bus is used for address. For MCU it is used only as an input address bus. For Blitter it is used as input address bus when it is a bus slave or as output address bus when it is a bus master.
122,127, 134,142, 176,169, 184,187, 11,15,23, 25,64,69, 91,94	D0-D15	I/O	This 16 bit bus is used for data.
186	AS-	I/O	Address strobe indicates that there is a valid address on the address bus. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.
171	UDS-	I/O	Upper data strobe controls the flow of data on the data bus together with LDS- and R/(W)-. For MCU it is an input. For Blitter it is an input when it is a bus slave or an output when it is a bus master.

Pin	Signal	Type	Description
43	R8006-	Output	Control line to enable reading I/O address FF8006.
113	FPUCS-	Output	FPU Chip Select.
120,114, 97,96,84, 77,61,39, 10,189, 149	MAD0-10	Output	DRAM address bus.
46	WE-	Output	DRAM write enable.
18,21	RAS0- RAS1-	Output	DRAM row address select lines.
22,62	CAS0H- CAS1H-	Output	DRAM CAS HIGH select lines.
70,83	CAS0L- CAS1L-	Output	DRAM CAS LOW select lines.
74	RAMH	Output	Address select control to the VIDEO SHIFTER to select the low or high DRAM word in 16 bit video bus. 0 - select the low word.
75	RTCCS-	Output	Real-time clock chip select.
76	RTCAS-	Output	Real-time clock address strobe.
85	RTCDS-	Output	Real-time clock data strobe.
89	SCCAB	Output	SCC Channel select.
165	SCCRD-	Output	SCC read signal.
164	SCCWR-	Output	SCC write signal.
88	SCCIACK-	Output	SCC interrupt acknowledge.
87	SCCWAIT-	Input	Active low input pin to support SCC.
115	BGO	Output	BGO used for arbitration daisy chaining.
86	TEST	Input	Test pin.
163	KHZ500W	Output	Switched 500 KHz clock used for controlling 6850 that transmits keyboard data.
96	POR	Input	Power on reset.
99	TEST2	Input	Test 2 pin.
	VDD	Input	Five power lines. Connected to 5V.
	GND	Input	Five ground lines.

2.1.6 DMA Support

The FALCON030 system contains a DMA controller which provides three channels of DMA for the computer. The ACSI DMA channel from the ST product line is fully contained and has been modified slightly to accommodate a 5380 SCSI controller as well as the AJAX FDC. A record and playback DMA channel for digital sound data are also contained in this chip. The playback channel is compatible with the existing eight bit stereo and mono modes from the STE and TT products and has sixteen bit stereo added. For audio DMA to take place, the memory controller inside the SDMA IC is programmed with the starting and ending address of the RAM buffer.

The DMA controller is set up to select the source and the number of 512 byte blocks to transfer, and then the FDC or external peripheral is given the command to send or receive data. The entire block of data is then transferred to or from memory without intervention by the CPU. The FDC or peripheral generally asserts its interrupt line to signal the completion of the transfer (and the availability of status information).

2.1.6.1 DMA Pin and Signal List

Pin	Signal	Type	Description
138,139, 140	FC0-FC2	I/O	68030 bus function code. These lines are normally inputs. They become outputs during DMA when the 68030 bus is granted. Only values of 5 and 6 (supervisor program and data) will allow I/O access. A value of 5 is output during DMA.
30,28,27, 26,25,24, 22,21,20, 18,17,15, 14,13,12, 11,10,8,7, 6,5,4,3	A1-A23	I/O	68030 bus address. These lines are normally inputs. They become outputs during DMA when the 68030 bus is granted. They are used to select registers during I/O and to address memory during DMA.
136,135, 134,132, 131,130, 129,128, 126,124, 123,122, 121,119, 118,117	D0-D15	I/O	68030 bus data. These lines are inputs for I/O writes and DMA reads and outputs for I/O reads and DMA writes. They are used for data transfer between the chip and the 68030 bus.
36	AS-	I/O	68030 bus address strobe. This line is an input during I/O and an output during DMA. It is used to qualify the value on the address bus.
35	LDS-	I/O	68030 bus lower data strobe. This line is an input during I/O and an output during DMA. It is used to qualify the data on data lines D0-D7.
34	UDS-	I/O	68030 bus upper data strobe. This line is an input during I/O and an output during DMA. It is used to qualify the data on data line D8-D15.
33	R/W	I/O	68030 bus read write. This line is an input during I/O and indicates a read of the chip when high and a write to the chip when low. This line is an output during DMA and indicates a read of the bus when high and a write to the bus when low.

Pin	Signal	Type	Description
38	DTACK-	I/O	68030 bus data acknowledge. This line is an output during I/O and indicates to the 68030 bus master that the current cycle can be terminated. During DMA this line is input to determine when to terminate a DMA cycle.
39	BERR-	Input	This signal is used to terminate a DMA cycle when the system detects a bus error. It is provided to prevent system lockup when a bus error occurs during DMA.
40	BR-	Output	This output is driven low when the 68030 bus is needed to perform DMA cycles.
41	BGI-	Input	A low on this input indicates that the 68030 bus is granted and that the chip can assume control of the bus at the completion of the current cycle, if one is in progress, or immediately.
43	BGO-	Output	This output is provided to support a daisy chain on the bus grant line to arbitrate multiple bus requests. When the chip is not requesting the bus, this output is driven to match the BGI- input else it is driven high (inactive).
44	BGA-	I/O	This output is driven low when the chip assumes the bus after the request grant handshake. When DMA operations have been completed and the chip releases the bus, this line is driven high then tri-stated.
45	RESET-	Input	A low on this input resets the chip and clears any current operational mode.
76	UWD	Output	This output is the data signal of the three wire MicroWire bus.
75	UWC	Output	This output is the clock signal of the three wire MicroWire bus.
74	UWEN-	Output	This output is the enable signal of the three wire MicroWire bus.
58	SMCLK	Input	This input is the master timing clock for the sound DMA channel.
32	BMODE	Input	This input is driven by the Bus Master. It is low for 68030 Bus Masters and high for 68000 Bus Masters.
70	PLYDATA	Output	Serial sound data to DSP Connector.
71	PLYCLK	Output	Clock signal for PLYDATA. It is controlled by the receive matrix.
69	PLYSYNC	I/O	This signal is an output when in continuous clock mode, and an input when in gated clock mode.

Pin	Signal	Type	Description
67	RECDATA	Input	This is the sound data supplied by an external device connected to the DSP. This signal can be fed to one of four devices. DMA In, DSP RX, Conn RX, or Internal DAC.
68	RECCLK	Output	This is the clock signal for RECDATA.
65	RECSYNC	I/O	This signal is an output when in continuous clock mode, and an input when in gated clock mode.
59	SCLOCK	Output	This is the master clock signal for the CODEC. It has two sources. The internal 25.175MHz for 50kHz samples, and the EXT_CLOCK supplied on the DSP connector.
62	ASCLK	Output	This is the serial clock for ASDIN and ASDOUT.
61	ASSYNC	Output	This is the bit and frame sync information for the CODEC. Its format is a two-bit wide pulse every 32-bits. The two-bit wide pulse occurs every 256 ASCLKs.
63	PSGN	Input	This is the serial data from the CODEC. It is sampled on the falling edge of ASCLK.
64	ASDOUT	Output	This is the serial data for the DAC. ASDOUT changes on the falling edge of ASCLK.
2	SINT	Output	This output is low when sound DMA is active and high otherwise. It will make a high to low transition at the beginning of a frame of sound data and a low to high transition at the end of the frame. This signal can be programmed to come from either the record or play channels.
142	SCNT	Output	This output is similar to SINT but is wider.
72	TEST	Input	When this input is high, the ACSI sector count can be read in the high byte of the ACSI status register. Also a low to high transition on this signal increments the sound DMA address counters and the ACSI sector prescale and count. This pin should be tied low for normal system operation.
141	DSKIRQ-	Output	FDINT high or HDINT- low make this output low.
77	FDINT	Input	This input affects DSKIRQ- only.
78	HDINT-	Input	This input affects DSKIRQ- only.
79	FRQ	Input	Active high DMA request from the FDC.
80	FCS-	Output	Active low chip select to the FDC.
83	HRQ	Input	Active high DMA request from the SCSI controller.
84	HCS-	Output	Active low chip select to the SCSI controller.

Pin	Signal	Type	Description
84	HCS-	Output	Active low chip select to the SCSI controller.
82	ACK-	Output	Active low DMA acknowledge to the SCSI controller.
86,87,88, 89,91,92, 93,94	CD0-CD7	I/O	Data bus for the FDC and SCSI controller.
98,97,96	CA0-CA2	Output	Register address to the and SCSI controller. Used to select FDC or SCSI controller registers during I/O.
100	CRW	Output	A high means transfer from the FDC or SCSI controller. A low means transfer to the FDC or SCSI controller.
99	CRW-	Output	The inverse of CRW.
101	DISKCHNG	Input	Status input for the floppy density select register.
102,103	MODE1 MODE2	Output	Status outputs for the floppy density select register.
114,115	MDET1 MDET2	Input	Status inputs for the floppy density select register.
104	CLK32I	Input	Feedback for the 32 Mhz oscillator.
105	CLK32O	Output	32 Mhz oscillator output.
106	CLK8	Output	Free running 32 Mhz clock divided by four.
113	CLK2	Output	Free running 32 Mhz clock divided by 16.
112	FCCLK	Output	32 Mhz clock divided by 1, 2, or 4 as selected by the floppy density select register.

2.1.7 Real-Time Clock

The FALCON030 system includes a Real-time Clock chip. When the system is powered on the real-time clock is powered by the main PCB power supply. In the event of a power failure, or when the system is powered off, the real-time clock is powered by a 3.6v lithium battery.

This allows the date, time, and configuration data to be maintained even when there is no power to the unit. 50 bytes of battery backed-up RAM is also provided for storing diagnostic and configuration data.

The real-time clock provides time of day (down to one second resolution) and date. The RTC contains an integrated battery and crystal. The chip is accessed through two consecutive word ports. The first word is a write-only port used to set the real-time clock chip address desired. The second word is the read-write data port.

When doing a write to a clock chip register, a double word write can be performed. The first word would set the address, and the second word would load the data.

2.1.7.1 Real-Time Clock Pin and Signal List

Pin	Signal	Type	Description
1	MOT	Input	This signal is tied high to select Motorola bus timing.
4-11	AD0-7	I/O	These are the multiplexed address data pins for the Real-Time Clock.
13	CS-	Input	This signal is used to select the Real-Time Clock.
14	AS	Input	This signal is used to latch addresses into the Real-Time Clock.
15	R/(W)-	Input	This signal is used to select data flow direction to the static RAM. A high selects a read operation. A low selects a write operation.
17	DS-	Input	This signal is used to latch data to or from the static RAM.
18	RESET-	Input	This signal is used to reset the RTC.
19	IRQ-	Output	This signal is used to send an interrupt to the system.
23	SQW	Output	This pin is not connected in the FALCON030 system.
24	Vcc	Input	+5V Power to RTC.
12	GND	Input	Ground for RTC.
16,20,21, 22,23	N/C	——	No Connect.

2.1.8 System Timing and Bus Control

There are six system resources that use the system memory separate from the microprocessor. In order of highest to lowest priority these are:

- Expansion Bus (optional using CPU/BGO)
- Video
- DMA
- Refresh
- Blitter (Graphics coprocessor inside COMBO IC)
- Expansion Bus (using daisy-chained BG)

Only two of these arbitrate for the system bus in a normal manner. These are the DMA and Blitter. The DMA chip which resides in the FALCON030 system contains the bus arbitration logic which arbitrates for either DMA disk transfers or DMA sound accesses. DMA arbitration has a higher priority than does the Blitter.

Video accesses in the system are done in Page Mode. Any video request for memory access will interrupt other DRAM access cycles, whether they are microprocessor, DMA, or Blitter, by inserting wait states into the current bus cycle. This is accomplished by holding off the DTACK signal. While the current cycle is in wait states, the memory bus is used for the video access. When the video cycle terminates, the DTACK signal is asserted and the current cycle is allowed to complete. Refresh cycles operate in the same manner.

2.1.8.1 68000 Bus Decode PAL U68

PAL U68 is used to generate Bus Grant for 68000 type devices. It also generates the BMODE signal used to inform the SDMA and COMBO IC that a 68000 type device is accessing the bus. 68000 type devices typically require an extra clock cycle, as opposed to 68030 devices, to complete strobe and handshaking signals. The DSP data strobe signal is also generated by this PAL.

2.1.8.2 68000 Bus Decode PAL U63

PAL U63 is used to generate the Expansion Data, Bus Error, and Data Transfer Acknowledge signals to the system. It also generates the Data Transfer Size and Acknowledge 1 signal.

2.1.8.3 68000 Bus Decode PAL U62

PAL U62 is used to generate 68000 compatible Upper and Lower Data Strobes (UDS, LDS), Valid Memory Address (VMA), Read/Write (RW), and Size 1 (SIZ1) bit.

2.1.8.4 68000 Bus Decode PAL U67

PAL U67 decodes the address for the DSP (56001) and genrates a partial DSP decode.

2.1.8.5. 68000 Bus Decode GAL U44

GAL U44 generates DSP Chip Select, Hardware Acknowledge, Mfp Interrupt Enable Out, Interrupt Acknowledge, Mfp Interrupt, and Data Size And Transfer Acknowledge 0.

2.1.9 Configuration Switch

Two configuration switches are provided for the enabling or disabling of hardware options on the main logic board. The switches are 8-bit DIP type and are located at U56 and U57.

NOTE: It is recommended that these switches not be changed as problems could result from their improper setting.

The values of these switches is as follows:

U56

Segment	Function
1	On = 1 Wait State DRAMs OFF = 0 Wait State DRAMs
2	On = 32-bit Video Bus Off = 16-bit Video Bus
3-4	Off Off = 0 Wait State ROMs Off On = 1 Wait State ROMs On Off = 2 Wait State ROMs On On = Reserved
5-6	Not Used
7-8	Not Used

U57

Segment	Function
1-4	Not Used
5	Off = Quad Density Floppy On = Don't Care
6	Off = AJAX Installed (1.44MB) On = 1772 Installed (720K)
7	Off = No DMA Sound Hardware On = DMA Sound Hardware Installed

2.2 AUDIO/VIDEO SUBSYSTEM

2.2.1 Video System Overview

The video subsystem in FALCON030 is composed of five major components. These are as follows:

- Video RAM (Dual-purpose System and Video)
- Interrupt and Data Load Control (COMBO)
- Video Shifter (VIDEL)
- Digital to Analog Converter (DAC)
- NTSC/PAL Encoder (1377)

The FALCON030 Video Subsystem extends the existing STE video modes. Video can be generated in ST compatible modes as well as VGA, True Color, and Programmable modes. Functionality has been enhanced by the ability of the subsystem to access video memory on any even word boundary. There is an RF modulator on-board to facilitate the direct connection to TV. Video also has the capability of being GENLOCKed for sync to external video timing sources. The monitor connector supplied with the system allows for the connection of ST color and ST monochrome monitors in addition to VGA type monitors.

The video modes supported by the system are as follows:

ST Modes

Resolution	Bit Planes	Colors	Palette Colors
320 X 200	4	16	4096/262,144
640 X 200	2	8	4096/262,144
640 X 400	1	2	4096/262,144

VGA Mode

Resolution	Bit Planes	Colors	Palette Colors
640 X 480	8	256	262,144

True Color

Resolution	Bit Planes	Colors	Palette Colors
320 X 200	15	32,768	1 Bit GENLOCK
320 X 200	16	65,536	No GENLOCK

Programmable

Resolution	Bit Planes	Colors	Palette Colors
X x Y	1,2,4,8	2,4,16,256	262,144

2.2.1.1 Video RAM

Video RAM is shared as dual-purpose memory with the rest of the FALCON030 system. The physical screen origin located at the top left corner of the screen is the start of mapped display memory.

Display memory is configured as 1, 2, 4, or 8 logical planes that are interwoven as 16-bit words into contiguous memory to form one physical plane starting at any even-word boundary.The size of this plane will depend on the video resolution and the number of colors selected. For example, 320 X 200 4 color mode would require a 32,000 byte plane.

2.2.1.2 Interrupt and Data Load Control (COMBO)

The COMBO IC is responsible for handling the interrupts generated by the VIDEL IC, and the loading of DRAM data into the video chip's input buffer. COMBO receives the interrupt signals VINT for VSYNC and HINT for HSYNC. A request for video data to be loaded into the video RAM buffer within the VIDEL IC is generated to the COMBO IC by the VREQ signal, and DRAM data is loaded into the video chip's input buffer via the VLD signal from the COMBO IC.

The starting address of display memory is placed in the COMBO IC's Video Base High, Video Base Mid, or Video Base Low Address registers by the Operating System or application. This register is loaded into the Video Address Counter (High/Mid/Low) in the COMBO IC at the beginning of each frame. The Address Counter is incremented as the Bitmap planes are read. COMBO then loads the VIDEL IC with Bitmap info 32-bits at a time.

2.2.1.3 Video Shifter (VIDEL)

The COMBO IC will load Bitmap planes into the VIDEL IC video buffer 32-bits at a time, except in XGA mode. The video shifter then loads the video shift register where one bit from each plane is shifted out and collectively used as the index to a specific STE or SP (FALCON030) palette register There are 16 word-wide color registers which comprise the STE palette and 256 double word-wide registers in the SP palette.

Each palette is programmed for 12 bits of color in STE mode, four for each red, green, and blue, or 18 bits of color in SP mode, 6 for each red, green, and blue. Therefore there are 16 x 16 x 16 or 4096 colors possible in STE mode, and 64 x 64 x 64 or 262,144 colors possible in SP mode. In monochrome mode, the color palettes are bypassed and instead provided with an inverter for inverse video controlled by bit 0 of palette register 0.

The VIDEL IC also has the ability to accept vertical sync and video clock. To inject a system clock ground pin 16 (EXT) on the monitor connector and then inject the clock into pin 15 (GENLOCK INPUT).

The internal frequency of this clock is 32.215905 MHz (NTSC) and 32.084988 MHz (PAL). VIDEL also includes the circuitry necessary to interface a light gun or pen plugged into Joystick 0. The current position that the gun or pen is pointing to is reported by these registers.

The position is accurate to within (X direction only):

- 4 Pixels in 320 x 200 Mode
- 8 Pixels in 640 x 200 Mode
- 16 Pixels in 640 x 400 Mode

Accurate to 1 pixel in the Y direction in all modes. Accuracies do not account for the quality of the light gun or pen. Note that the X position is given in pixels for 320 x 200 only. In order to get correct results in 640 x 200 mode this number needs to be shifted left one bit and in 640 x 400 modes this number needs to be shifted left two bits.

2.2.1.4 Video Digital to Analog Converter (DAC)

The Video DAC is used to take digital TTL input data from the VIDEL IC and convert it to analog RGB output. Inputs of 6-bit color info from the VIDEL are supplied to the DAC via the R2-R7, G2-G7, and B2-B7 inputs. The DAC then outputs analog R, G, and B to the monitor connector.

2.2.1.4.1 Video Digital to Analog Converter Pin and Signal List

Pin	Signal	Type	Description
40	COM	Input	Tied high in the FALCON030 system to select internal digital channel to output amplifier.
4-1,44-41	G0-7	Input	Eight bit green input data from VIDEL.
36-29	B0-7	Input	Eight bit blue input data from VIDEL.
12-5	R0-7	Input	Eight bit red input data from VIDEL.
37	RC	Input	Tied high in the FALCON030 system to select binary coding on R and B data.
25	BEXT	Input	Auxiliary blue input. Not connected in the FALCON030 system.
22	GEXT	Input	Auxiliary green input. Not connected in the FALCON030 system.
19	REXT	Input	Auxiliary red input. Not connected in the FALCON030 system.
18	ROUT	Output	Analog red output to monitor connector.
21	GOUT	Output	Analog green output to monitor connector.
24	BOUT	Output	Analog blue output to monitor connector.
38	CLK	Input	Clock input.
15,26	AVcc	Input	Chip power input.

2.2.1.5 NTSC/PAL Encoder (1377)

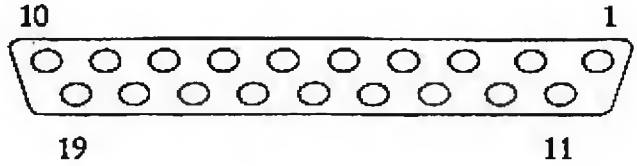
The 1377 encoder is used in the system to convert baseband RGB and sync signals into a composite TV signal.

2.2.1.6 VIDEL Pin and Signal List

Pin	Signal	Type	Description
60,59,57, 55,50,39, 35,33,32, 31,29	A1-A11	Input	These are the 11 LSB of the CPU address bus.
19,20,21, 24,26,28, 34,36,37, 38,40,41, 42,43,48, 49	D0-D15	I/O	This is the CPU data bus.
78-84,87-89,92-85	MD0-31	I/O	This is the 32 bit DRAM data bus. Data is read from this bus when the DRAM is read. Data is written onto this bus when the DRAM is written.
18,17,13, 2,11,9,51, 52,53,54, 56,58,64-68,72	R0-R5 B0-B5 G0-G5	Output	These are the 3x6 digital RGB outputs.
10	DOTCK	Output	This is the clock for the DAC.
8	MONO	Output	This is the monochrome output when not in XGA. In CONTROL XGA mode it is the pixel control.
96	COLOR	Output	This is a timing signal for composite video generation for NTSC TV.
62	CSYNC	Output	This signal is the composite sync output.
47	VREQ	Output	This is the video request active high output.
44	CLK32	Input	This is a 32 Mhz clock input. Used in non VGA cases.
73	CLK25	Input	This is a 25-Mhz clock input for VGA cases.
14	EXTCLK	Input	This is the external Genlock clock input.
6	VSYNC-	I/O	This is the vertical sync signal. It is programmable as input or out.
114	TEST.		
3	HSYNC-	I/O	This is the horizontal sync signal. It is programmable as input or out. In case of TV it contains the full interlace support.

Pin	Signal	Type	Description
101	HINT-	Output	This is the horizontal display enable signal used for Hsync interrupt generation.
97	VINT-	Output	This is the vertical display enable signal used for Vsync interrupt generation.
7	R/(W)-	Input	This is the CPU R/W input signal. It is used to access the internal registers including CLUT. When high the registers are read to the CPU. When low the registers are written with data from the CPU.
25	VCS	Input	This is the chip select active high input. It selects the video chip for CPU read/write accesses (according to R/W) to/from the video chip internal registers or CLUT. It is controlled by the CPU DS.
66	VLD	Input	This signal informs the video chip that the data read from the DRAM is to be loaded into the video INPUT BUFFER.
22	RDAT-	Output	This active low signal enables the data read from the DRAM into the CPU data bus to enable CPU reading from the DRAM.
23	WDAT-	Output	This active low signal enables the CPU data bus into the DRAM data bus to enable CPU writing into DRAM.
70,71	CAS0- CAS1-	Output	These are the SIMMs active low CAS signals. They are ORed in the video chip and used to latch the DRAM data into the INPUT BUFFER.
2	PEN-	Input	This is the Light/gun pen input.
4	LOWP	Input	Low Power pin. Can be used to disable the clocks. It is grounded in normal applications.
5	RAMH	Input	This is an address control signal from COMBO to select the high or low DRAM word in 16 bit video bus. 0 selects low word.
85	ODD_EVEN	Output	An output pin to indicate odd/even video frames. 0 - EVEN.
86	DE	Output	Display Enable.
1	RESET	Input	Reset to VIDEL chip.
	DGND	Input	Digital ground pins.
	DVcc	Input	Digital power pins.
119	EXT	Input	Used to turn on the external Genlock logic.
112	TN	Input	Used for VLSI parametric testing.

2.2.1.7 Monitor Connector Pin List



1	Red	11	Ground
2	Green	12	Composite Sync
3	Blue	13	Horizontal Sync
4	Mono Out	14	Vertical Sync
5	Ground	15	Externa Clock Input (GENLOCK)
6	Red Return (GND)	16	EVEN_ODD
7	Green Return (GND)	17	+12 Volts for PERITEL
8	Blue Return (GND)	18	Video Master Control Bit 1
9	Audio In	19	Video Master Control Bit 2
10	Ground		

2.2.2 Audio Subsystem

The FALCON030 architecture extends the music subsystem presently available on the ST/MEGA computers. The FALCON030 mixes the output of the existing ST PSG sound system with a new DMA-driven dual-channel A-toD, D-to-A subsystem (Codec device). The FALCON030 combines these two sources for simple beeps, and can be connected to an external stereo amplifier for high-fidelity sound. In addition the resulting audio is sent to an on-board speaker which can be turned off with an general purpose bit from the PSG.

2.2.2.1 Programmable Sound Generator

The ST sound system using the General Instruments AY-3-8910/Yamaha YM-3439 Programmable Sound Generator is present in the FALCON030 system. The YM-3439 Programmable Sound Generator produces music synthesis, sound effects, and audio feedback.

With an applied clock input of 2 MHz, the PSG is capable of providing a frequency response range between 30 Hz (audible) and 124 KHz (post-audible). The generator places minimal amount of processing burden on the main system (which acts as the sequencer) and has the ability to perform using three independent voice channels. The three sound channel outputs are mixed, along with Audio In, and sent to the CODEC IC for processing. The PSG also provides the speaker gate for the internal speaker.

2.2.2.2 DMA Sound

The FALCON030 also includes a new DMA-driven sound subsystem that allows the playback or synthesis of complex waveforms at a variety of sampling rates. This feature is supported by the new Codec device which is driven from the new DMA device (same IC that controls the disk DMA cycles).

Sound in the form of digitized samples is stored in system memory. These samples are fetched from dual-purpose memory by the SDMA IC (transparent to the processor) and provided to digital-to-analog converters (DAC's) in the Codec device at a constant sample frequency specified by the user. The outputs of the DAC's are then low pass filtered into a walkman type, micro-stereo connector and to the on-board speaker.

Two channels are provided. They are intended to be used as the left and right channels of a stereo system when using the raw audio outputs from the machine. They are mixed together when fed to the on board speaker or monitor speaker. A MONO mode is provided which will feed the same data to both channels simultaneously. The only restriction placed on MONO mode is that there must be an even number of samples.

2.2.2.3 Codec IC

The Codec IC in the FALCON030 system is connected through a serial protocol to provide both an Analog to Digital (ADC) and Digital to Analog (DAC) function for in the 16-bit stereo sound system. The Codec is strapped so that the ADC operates as a conventional oversampling ADC producing stereo data at the output. The DAC operates as a conventional oversampling single bit DAC.

A serial interface is used to connect the Codec IC to the system. It is made up of a data line in, a data line out, a clock line, and a syncchronization input. Serial data from the SDMA IC to the CODEC consists of interleaved volume, control, and 16-bit stereo sound data. Volume control is achieved by changing the interleaved volume data values.

2.2.2.3.1 Codec Pin and Signal List

Pin	Signal	Type	Description
1	SSYNC	Input	The Serial Sync Input signal is used to indicate the start of a word or frame of transmissions via the serial interface.
2	RESET-	Input	The Reset input signal is used to reset the CIDC IC.
3	CLKIN	Input	The CLKIN input signal is used as the master clock of the CODEC IC. The D to A and A to D converters are driven by this input.
4	DVcc	Input	This is the power supply voltage for the CODEC IC.
5	DGND	Input	This is the ground for the CODEC IC.

Pin	Signal	Type	Description
13	PON-	Input	The Low Power Mode input signal is used to switch the CODEC to low power mode. This pin is tied to Vcc in the Falcon030.
15	ROUT	Output	The Right Analog Output pin is the right channel analog output signal.
16	LOUT	Output	The Left Analog Output pihn the left channel analog output signal.
18	POMCR	—	The Capacitor Connection pin is used for the outer feedback loop of the pulse density modulator for the right channel. It is tied to the REFBUF pin.
19	POMCL	—	The Capacitor Connection pin is used for the outer feedback loop of the pulse density modulator for the left channel. It is tied to the REFBUF pin.
20	REFBUF	—	The Buffered Internal Analog Ground pin is the buffered signal analog ground pin for the pulse density modulator capacitors.
21	REFBYP	—	The Internal Analog Ground pin is the clean analog ground pin for the analog input and output connectors.
22	REFGND	—	The Reference Analog Ground pin is the ground pin that serves as a clean ground for the CODEC IC.
23	AGND	—	The Analog Ground pin is used as an analog ground for the CODEC IC.
24	AVcc	Input	The Analog Supply Voltage pin is used to supply power to the analog circuitry of the CODEC IC.
25	RIN1	Input	The Right Analog Input Channel 1 signal is fed to this pin.
26	RIN2	Input	The Right Analog Input Channel 2 signal is fed to this pin.
27	LIN1	Input	The Left Analog Input Channel 1 signal is fed to this pin.
28	LIN2	Input	The Left Analog Input Channel 2 signal is fed to this pin.
29	MDSEL	Input	The Mode Select Input signal is used to select additional serial formats when pulled high. It is tied to ground in the Falcon030 system.
30	SBF2	Input	The Subframe Input 2 pin is used to determine what subframe the CODEC IC will be active. This pin is grounded in the Falco030 system.

Pin	Signal	Type	Description
31	SBF1	Input	The Subframe Input 1 pin is used in conjunction with the Subframe Input 2 pin to determine what subframe the CODEC IC will be active. This pin is grounded in the Falco030 system.
32	TESTEN	Input	The TestMode Enable pin is used to seitch the CODEC IC into test mode. This pin is grounded in the falcon030 system.
33-36	DI1-DI4	Input	The Digital Input 1-4 pins are used to supply digital data to the CODEC IC. These pins are grounded in the Falcon030 system.
33-40	DO1-DO4	Output	The Digital Output 1-4 pins are used to supply digital data from the CODEC IC. These pins are not connected in the Falcon030 system.
41	TEST2	Input	The Test 2 pin is used for test mode sychronization. It isnot connected in the Falcon030 system.
42	SDIN	Input	The Serial Data Input pin is used to input serial digital data to the CODEC IC.
43	SDOUT	Output	The Serial Data Output pin is used to output the analog to digital signal according to the serial interface format.
44	SCLK	Input	The Serial clock input pin is used 5to define the bit clock for theserial interface. It latches the data in on thè SDIN line, and out on the SDOUT line.

2.3 I/O SUBSYSTEMS

The FALCON030 architecture supports the following device subsystems:

- IDE Hard Disk Interface.
- External SCSI II Hard Disk Port.
- Floppy disk interface sharing the ST ACSI DMA channel.
- Serial port and an external LAN port connected to SCC controller.
- A Centronics parallel printer port driven by the Yamaha YM-3439 sound chip.
- An ST/MEGA compatible intelligent keyboard, mouse, and joystick interface.
- Option for interfacing to the new Atari Universal Keyboard Controller.
- A port supporting application and diagnostic cartridges.
- Two controller ports for additional joysticks as well as light pen/gun and paddle controllers.

2.3.1 SCSI II Interface

The external hard disk drive interface is provided through a standard 5380 NCR SCSI Controller. Transfers can take place at up to 2Mbytes/second. The controller interfaces to the system through the SDMA IC.

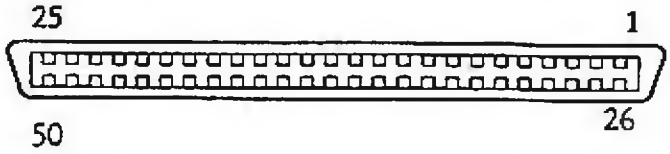
2.3.1.1 5380 SCSI Controller Pin and Signal List

Pin	Signal	Type	Description
37-41,43-44,1	DB0- to DB7-	I/O	8-bit SCSI data bus. During arbitration these lines contain the SCSI ID numbers of all devices arbitrating for the SCSI bus. During selection, these lines contain the ID number of the device which has been selected.
35	DBP-	I/O	SCSI data bus parity bit.
5	SEL-	I/O	The Select signal is asserted by the initiator to select a target. It can also be asserted by the target when reselecting it as an ititiator.
4	BSY-	I/O	Busy is asserted when the SCSI bus is active.
33	ACK-	I/O	Acknowledge is asserted by the initiator during information transfer phases in response to REQ- asserted by the target.
6	ATN-	I/O	Attention is asserted by the intiator after the successful selection of a target.
7	RST-	I/O	When active this signal indicates a SCSI bus reset condition.
32	I/O-	I/O	I/O is controlled by the target device and indicates the direction of data transfer. When low the direction of data flow is to the initator.

Pin	Signal	Type	Description
30	C/D-	I/O	Control/Data is sent by the target to indicate that control or command information is on the SCSI bus.
29	MSG-	I/O	Message is controlled by the target device and indicates a message phase of operation.
34	REQ-	I/O	The Request signal is asserted by the target device to begin the handshake needed to transfer a byte of data over the bus. The REQ- signal is negated upon the receipt of an ACK- signal by the initiator.
17	CS-	Input	Chip Select enables reading or writing from the 5380.
9	DRQ	Output	DMA Request is used to request DMA service from the DMA controller.
8	IRQ	Output	Interrupt Request is used to send an interrupt to the microprocessor.
19	IOR-	Input	The I/O Read signal is used to read the controller's registers.
13	READY-	Output	The READY signal can be used as an alternate DRQ device. This pin is not connected in the FALCON030 system.
11	DTACK-	Input	DMA Acknowledge is used to enable reading or writing of the SCSI controller's internal registers.
10	EOP-	Input	The End Of Process signal is used to indicate that a DMA transfer is to be concluded.
7	RESET-	Input	The Reset signal is used to reset the SCSI controller.
18	IOW-	Input	The I/O Write signal is used to write information to the SCSI controller's registers.
14-16	A0-2	Input	Address lines 0-2 are used to select the internal SCSI controller register which is to be accessed.
28-24,22-20	D0-7	I/O	Data lines 0-7 are the microprocessor data bus.

2.3.1.2 External SCSI Connector Pin List

The SCSI interface uses a 50 pin connector with the following pin assignment:



Pin	Signal	Pin	Signal
1-10	Ground	37	No Connect
11	+5 Volts	38	+5 Volts 1A Fuse
12-14	No Connect	39	No Connect
15-25	Ground	40	Ground
26	SCSI 0	41	ATN
27	SCSI 1	42	Ground
28	SCSI 2	43	Busy
29	SCSI 3	44	Acknowledge
30	SCSI 4	45	Reset
31	SCSI 5	46	Message
32	SCSI 6	47	Select
33	SCSI 7	48	Code/Data (C/D)
34	Parity	49	Request
35-36	Ground	50	I/O

2.3.2 Floppy Disk (FDD)

The FALCON030 floppy disk subsystem is designed around the AJAX Floppy Disk Controller supporting one floppy disk drive. It is a higher speed version of the 1772 and supports 1.44Mb (formatted) capacity drives.

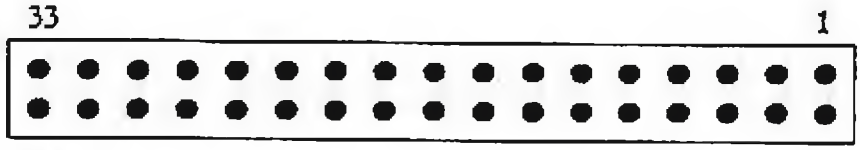
The subsystem interfaces to the dual-purpose RAM through the ACSI DMA controller, which is part of the SDMA IC. Commands and arguments are sent to the FDC by first writing to the DMA Mode Control Register to select the desired FDC register and then writing the data bytes. The standard floppy for the FALCON030 is the 3.5 inch floppy disk with the capacity of 1.44 Mbyte (formatted).

2.3.2.1 AJAX Pin and Signal List

Pin	Signal	Type	Description
1	CS-	Input	Chip Select is used to enable communications between the chip and the host interface.
2	R(W)-	Input	Read/Write- is used to control the direction of data from the internal registers in the device. A low enables a read of the registers, a high enables a write to the registers over the DAL0-7 lines.
3,4	A0,A1	Input	Address 0-1 are used to select the internal register in the device that is to be read or written.
5-12	DAL0-DAL7	I/O	The Data 0-7 lines are an 8-bit bus used to transfer data, commands, or status.
13	MR-	Input	Master Reset is used to reset the AJAX chip.
14	GND	Input	Ground for the AJAX chip.
15	Vcc	Input	Power Supply (+5V) for the AJAX chip.
16	STEP	Output	Step is used to step the read/write heads of the FDD.
17	DIRC	Output	Direction is used to select whether the FDD heads are stepped toward the center or out from the center of the FDD. A high causes the heads to step toward the center.
18	CLK	Input	Free running clock input.
19	RD-	Input	Read Data is the raw data line containing both clock and data pulses from the FDD.
20	MO	Output	Motor On is used to enable the spindle motor of the FDD.
21	WG	Output	Write Gate is used to enable writing to the FDD.
22	WD	Input	Write Data is the clock and data pulses to be written to the FDD.
23	TR00-	Input	Track 00 informs the AJAX chip that the FDD's heads are over track 0.
24	IP-	Input	Index Pulse tells the AJAX chip when the Index Hole on the Diskette has been encountered.
25	WPRT-	Input	Write Protect tells the AJAX chip that the diskette in the FDD is write protected.

Pin	Signal	Type	Description
26	DDEN-	Input	Double Density Enable is used selects FM or MFM operation of the FDD. A low is MFM.
27	DRQ	Output	Data Request is used to indicate that the internal data register is full on a read, or empty on a write.
28	INTRQ	Output	Interrupt Request is used to tell the host system that a command has been completed.

2.3.2.2 Internal Floppy Connector Pin List



Pin	Signal	Pin	Signal
1	Ground	2	Mode Select 1
3	Ground	4	Not Connected
5	Ground	6	Mode Select 2
7	Ground	8	Index Pulse
9	Ground	10	Drive Select 0
11	Ground	12	Not Connected
13	Ground	14	Not Connected
15	Ground	16	Motor On
17	Ground	18	Direction Select
19	Ground	20	Step
21	Ground	22	Write Data
23	Ground	24	Write Gate
25	Ground	26	Track 0
27	Ground	28	Write Protect
29	Media Detect 2	30	Read Data
31	Ground	32	Side Select
33	Media Detect 1	34	Disk Change

2.3.3 68901 MFP

A 68901 Multi-Function Peripheral (MFP) controller is used to provide system timers and an interrupt controller. The MFP is used in a way that is compatible with the ST.

2.3.3.1 Interrupt Control

Interrupts handled by the 68901 MFP are as follows:

- RS232 Ring Indicator Interrupt
- Sound Interrupt
- ACSI/FDD/IDE Interrupt
- MIDI Interrupt
- Keyboard/MIDI Interrupt
- DSP Interrupt
- Printer Acknowledge Interrupt
- Printer Busy Interrupt

2.3.3.2 68901 MFP Pin and Signal List

Pin	Signal	Type	Description
1	NC1	——	No Connect.
2	RXW	Input	Read/Write defines the current bus cycle as a read or write cycle. When high it is a read. When low it is a write.
3-7	RS1-5	Input	The Register Select bus bits are used to select an internal MFP register during a read or write cycle.
8	TC	Input	The Transmitter Clock input controls the serial bit rate of the transmitter within the MFP. It is tied to the Timer D output.
9	SO	Output	This is the USART serial data output line. This pin is not connected in the Falcon030 system.
10	SI	Input	This is the USART serial input data line. This pin is grounded in the Falcon030 system.
11	RC	Input	The Receiver Clock is used to control the bit rate of the receiver internal to the MFP. It is tied to the Timer D output.
12	Vcc	Input	Power to the 68901.
13	NC	——	No Connect.
14	NC	——	No Connect.

Pin	Signal	Type	Description
15	TAO	Output	Timer A Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
16	TBO	Output	Timer B Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
17	TCO	Output	Timer C Output is not connected in the FALCON030. This pin is not connected in the Falcon030 system.
18	TDO	Output	Timer D Output is tied to the TC and RC pins of the 68901 to provide rate timing for transmit and receive. The serial portion of the 68901 MFP is not used in the Falcon030 system.
19	XTAL1	Input	Crystal input for timers.
20	XTAL2	Input	Crystal input for timers.
21	NC	——	No Connect.
22	TAI	Input	Timer A Input is a control signal for the Timer A internal to the MFP. It is tied to the Sound Interrupt.
23	TBI	Input	Timer B Input is a control signal for the Timer B internal to the MFP. It is tied to the Display Enable Interrupt.
24	Reset	Input	The Reset signal is used to reset the 68901.
25	IO0	I/O	General Purpose Input 0 is used as an interrupt input for Printer Busy.
26	IO1	I/O	General Purpose Input 1 is used as an interrupt input for Printer Acknowledge.
27	IO2	I/O	General Purpose Input 2 is used as an interrupt input for the MIDI.
28	IO3	I/O	General Purpose Input 3 is used as an interrupt input for the DSP.
29	IO4	I/O	General Purpose Input 4 is used as an interrupt input for Keyboard/MIDI.
30	IO5	I/O	General Purpose Input 5 is used as an interrupt input for IDE/SCSI.
31	IO6	I/O	General Purpose Input 6 is used as an interrupt input for RS232 Ring Indicator.

Pin	Signal	Type	Description
32	IO7	I/O	General Purpose Input 7 is used as an interrupt input for Sound System.
33-35	NC	——	No Connect.
36	IRQ	Output	IRQ is used to alert the 68030 that an interrupt is pending.
37	IEO	Output	Interrupt Enable Out allows any device daisy chained off the MFP to signal an interrupt if no higher priority device is requesting an interrupt.
38	IEI	Input	Tied to ground unless expansion is used. Then it is tied to the IEO pin of the expansion MFP to signal no higher priority device is requesting an interrupt.
39	CLK	Input	Input clock for the MFP.
40	GND	Input	Chip ground.
41-48	D0-D7	I/O	8-bit data bus.
49	IACK	Input	Interrupt Acknowledge from the 68030.
50	DTACK	Output	Data Transfer Acknowledge signals completion of a data transfer phase of operation.
51	DS	Input	Data Strobe is used to latch data into the MFP.
52	CS	Input	Chip Select is used to enable the MFP for access.

2.3.4 8530 Serial Communications Controller (SCC)

The Falcon030 contains an 8530 Serial Communications Controller (SCC) that provides a dual channel, multi-protocol device that provides a serial port and network LAN port. The input/output of the serial port is routed to a DB-9P connector. The input/output of the LAN port is routed to a DB-8P connector.

The PCLK input to the SCC is rated at 8 MHz. The RTXCA and RTXCB input is provided with a 3.672 MHz clock. The TRXCA input comes from the LAN connector, and the TRXCB input is rated at 2.4576 MHz.

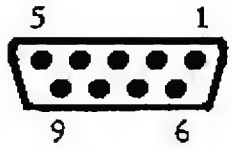
2.3.4.1 8530 Pin and Signal List

Pin	Signal	Type	Description
1-5,42-44	D0-D7	I/O	8-Bit data bus.
6	INT	Output	Interrupt Request from the SCC.
7	IEO	Output	Interrupt Enable Out is used to daisy chain several devices together. Normally it is tied to the IEI pin of the next device. It is not connected in the FALCON030 system.
8	IEI	Input	Interrupt Enable In is used to daisy chain to the next higher priority device. It is connected to +5V to indicate there is no higher priority device in the system.
9	INTACK-	Input	Interrupt Acknowledge is used to indicate that an active interrupt acknowledge cycle is taking place.
10	+5V	Input	+5 Volt power supply for the IC.
11	SCCWAIT	Output	SCC Wait Request is used to set up wait timing for CPU synchronization.
12	SYNCA	I/O	Synchronization A is used as an input or otput for channel A depending upon the mode of operation. In Asynchronous Receive Mode the pin acts as an input similar to CTS and DCD. In External Synchronization Mode this pin acts as an input and must be driven low to receive clock cycles after the last sync bit. In the Internal Synchronization Mode the pin is an output and only active during the part of the receive clock cycle in which sync characters are being received. This opin is tied to the DSRA signal.
13	RTXCA-	Input	Receive/Transmit Clock A is the clock signal for the receive/transmit circuit for channel A.
14	RXDA	Input	This is the serial data receive pin for channel A.
15	TRXCA	I/O	Transmit/Receive Clock Channel A is used to supply the transmit or reseive clock for channel A.
16	TXDA	Output	Transmit Data Channel A is used to transmit serial data on channel A.
17	P17	——	No Connect.

Pin	Signal	Type	Description
18	P18	——	No Connect.
19	DTR/REQA-	I/O	The Data Terminal Ready/Request Channel A signal is used to show the state of the DTR bit for channel A.
20	RTSA-	Output	The Request To Send Channel A signal is used to reflect the state of the Request To Send bitfor channel A.
21	CTSA-	Input	The Clear To Send Channel A reflects the state of the Clear To Send bit for channel A.
22	DCDA-	Input	The Data Carrier Detect Channel A is used to reflect the state of the DCD bit for channel A.
23	PCLK	Input	This siganl is used as the master SCC clock.
24	DCDB-	Input	The Clear To Send Channel A reflects the state of the Clear To Send bit for channel B.
25	CTSB-	Input	The Data Carrier Detect Channel A is used to reflect the state of the DCD bit for channel B.
26	RTSB-		The Request To Send Channel A signal is used to reflect the state of the Request To Send birfor channel B.
27	DTR/REQB-		The Data Terminal Ready/Request Channel A signal is used to show the state of the DTR bit for channel B.
28	NC	——	No Connect.
29	TXDB	Output	Transmit Data Channel A is used to transmit serial data on channel B.
30	TRXCB-	I/O	Transmit/Receive Clock Channel A is used to supply the transmit or reseive clock for channel B.
31	RXDB	Input	This is the serial data receive pin for channel B.
32	RTXCB-	Input	Receive/Transmit Clock A is the clock signal for the receive/transmit circuit for channel B.

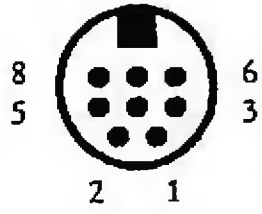
Pin	Signal	Type	Description
33	SYNCB-	I/O	Synchronization A is used as an input or otput for channel A depending upon the mode of operation. In Asynchronous Receive Mode the pin acts as an input similar to CTS and DCD. In External Synchronization Mode this pin acts as an input and must be driven low to receive clock cycles after the last sync bit. In the Internal Synchronization Mode the pin is an output and only active during the part of the receive clock cycle in which sync characters are being received. This opin is tied to the DSRB signal.
34	W/REQB-	——	No Connect.
35	GND	Input	Ground.
36	NC	——	No Connect.
37	D/C-	Input	Data/Control Select is used to select the type of information being transferred by the SCC. A high = data.
38	CE-	Input	This is the chip enable signal for the SCC.
39	A/B-	Input	This is the chaneel select input for the SCC.
40	WR-	Input	This signal is used to indicate a write operation.
41	RD	Input	This signal is used to indicate a read operation.

2.3.4.2 8530 Serial Port Pin and Signal List



Pin	Function
1	Carrier Detect (In)
2	Receive Data (In)
3	Transmit Data (Out)
4	Data Terminal Ready (Out)
5	Ground
6	Data Set Ready (In)
7	Request to Send (Out)
8	Clear to Send (In)
9	No Connect

2.3.4.3 SCC LAN Connector Pinout



Pin	Function
1	Output Handshake
2	Input Handshake
3	Transmit Data-
4	Ground
5	Receive Data-
6	Transmit Data+
7	(Reserved)
8	Receive Data+

2.3.5 Parallel Printer Port

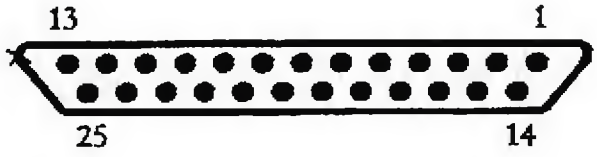
The FALCON030 architecture includes a bi-directional 8-bit parallel printer port that implements a subset of the Centronics standard.

This interface is through the General Instruments AY-3-8910 or Yamaha YM-3439 Programmable Sound Generator (PSG) chip. It is pinned out in a DB25S. The Centronics STROBE signal is generated from a PSG bit.

The Centronics BUSY and Printer Acknowledge signals from the printer connects to one of the parallel input lines of the MFP to permit interrupt driven printing. Eight bits of read/write data are handled through I/O port B on the PSG at a typical data transfer rate exceeding 4000 bytes/second.

2.3.5.1 Parallel Port Connector Pin List

The parallel port uses a DB 25 pin S connector with the following pin assignments:



Pin	Function	Pin	Function
1	Centronics Strobe	2	Data 0
3	Data 1	4	Data 2
5	Data 3	6	Data 4
7	Data 5	8	Data 6
9	Data 7	10	Acknowledge
11	Centronics Busy	12	Not Connected
13	Not Connected	14	Not Connected
15	Not Connected	16	Not Connected
17	Select In	18	Ground
19	Ground	20	Ground
21	Ground	22	Ground
23	Ground	24	Ground
25	Ground		

2.3.6 Keyboard Interface

The keyboard interface is completely compatible with the ST/MEGA computers. The keyboard is equipped with a combination mouse/joystick port and a joystick only port. The keyboard transmits encoded make/break key scan codes (with two key rollover), mouse/trackball data, joystick data, and time-of-day.

The keyboard receives commands and sends data via bidirectional communication implemented with a MC6850 Asynchronous Communications Interface Adapter (ACIA). All keyboard functions, such as key scanning, mouse tracking, command parsing, etc. are performed by a HD6301V1 8-bit microcomputer unit. (See the Atari, Intelligent Keyboard (ikbd) Protocol, February 26, 1985.)

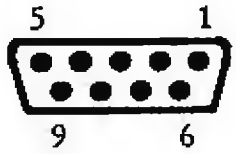
FALCON030 also has hooks to interface to the new Atari Universal Keyboard Controller. These hooks prevent data overrun both to and from the keyboard controller.

2.3.7 Mouse and Joystick Interface

The Atari two-button mouse is a mechanical, optomechanical, or optical mouse with the following minimal performance characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second, and maximum pulse phase error of 50%. The joystick is a four direction switch-type joystick with one fire button.

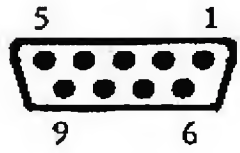
2.3.7.1 Mouse and Joystick Interface Connector Pin List

Mouse/joystick0 uses a DB9 pin P connector with the following pin assignment:



Pin	Function
1	Xb Pulse/ Up Switch
2	Xa Pulse/ Down Switch
3	Ya Pulse/ Left Switch
4	Yb Pulse/ Right Switch
5	Not Connected
6	Left Button/ Fire Button
7	Power
8	Ground
9	Right Button/ Joy1 Fire

Joystick1 uses a DB 9 pin P connector with the following pin assignment:



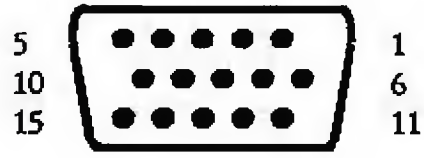
Pin	Function
1	Up Switch
2	Down Switch
3	Left Switch
4	Right Switch
5	Reserved
6	Fire Button
7	Power
8	Ground
9	Not Connected

2.3.8 Game Controller Ports

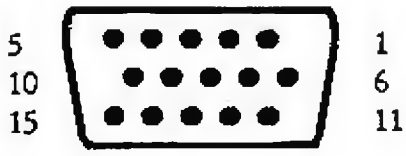
The FALCON030 system includes two STE compatible game controller ports which can be used for paddles, joysticks, or a light pen. These ports are enabled by the COMBO IC and interface directly to the data bus of the 68030.

2.3.8.1 Game Controller Pinout

Controller A



Pin	Function	Pin	Function
1	Up 0	2	Dn 0
3	LT 0	4	RT 0
5	Pad 0Y	6	Fire 0/Light Gun Pulse
7	+5 VDC	8	Not Connected
9	Ground	10	Fire 1
11	Up 1	12	Dn 1
13	LT 1	14	RT 1
15	Pad 0X		



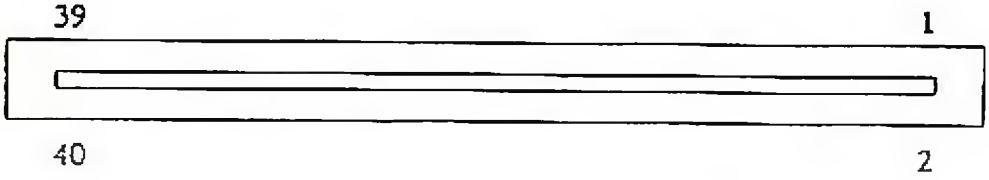
Pin	Function	Pin	Function
1	Up 2	2	Dn 2
3	LT 2	4	RT 2
5	Pad 1X	6	Fire 2
7	+5 VDC	8	Not Connected
9	Ground	10	Fire 3
11	Up 3	12	Dn 3
13	LT 3	14	RT 3
15	Pad 1Y		

2.3.9 ROM Cartridge

The FALCON030 cartridge port is fully compatible with ST cartridge. The cartridge is physically connected through a 40 pin card edge connector ROM cartridge slot. Cartridge ROMs are mapped to a 128K memory region starting at 0x00FA0000, extending to 0x00FBFFFF.

2.3.9.1 ROM Cartridge Connector Pin List

If not in a plastic housing, the cartridge must be installed with the chips facing down. The cartridge uses a 40 pin card edge S connector with the following pin assignment:



Pin	Function	Pin	Function
1	+5VDC	2	Power +5Vdc
3	Data 14	4	Data 15
5	Data 12	6	Data 13
7	Data 10	8	Data 11
9	Data 8	10	Data 9
11	Data 6	12	Data 7
13	Data 4	14	Data 5
15	Data 2	16	Data 3
17	Data 0	18	Data 1
19	Address 13	20	Address 15
21	Address 8	22	Address 14
23	Address 7	24	Address 9
25	Address 6	26	Address 10
27	Address 5	28	Address 12
29	Address 11	30	Address 4
31	ROM3 Select	32	Address 3
33	ROM4 Select	34	Address 2
35	Upper Data Strobe	36	Address 1
37	Lower Data Strobe	38-40	Ground

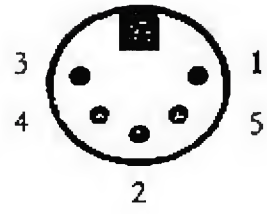
2.3.10 Musical Instrument Digital Interface (MIDI)

The MIDI allows the integration of the FALCON030 series with music synthesizers, sequencers, drum boxes, and other devices possessing MIDI interfaces. High speed (31.25 Kbaud) serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (the MIDI OUT also includes MIDI THRU data).

The MIDI communicates through the MC6850 Asynchronous Communications Interface Adapter (ACIA) to the system bus. The data transfer rate is a constant 31.25 Kbaud of 8-bit asynchronous data.

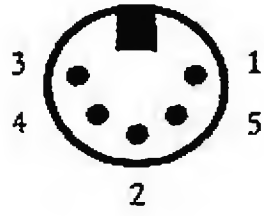
2.3.10.1 MIDI Connector Pin List

The MIDI OUT/THRU uses a circular DIN 5 pin S connector with the following pin assignment:



Pin	Function
1	Thru Transmit Data
2	Shield Ground
3	Thru Loop Return
4	Out Transmit Data
5	Out Loop Return

The MIDI IN uses a circular DIN 5 pin S connector with the following pin assignment:



Pin	Function
1	Not Connected
2	Not Connected
3	Not Connected
4	In Receive Data
5	In Loop Return

2.3.11 Digital Processor Interface (DSP)

The FALCON030 system includes a Digital Signal Processor (DSP) which can be used for complex audio and video processing. The DSP is located across the data and address buses of the 68030, and also has access to 32K of 24-bit, zero wait-state static RAM. The RAM can be used for information storage. Some of the various uses for the DSP would be sound and music synthesis, special sound effects, and 3D graphics modeling.

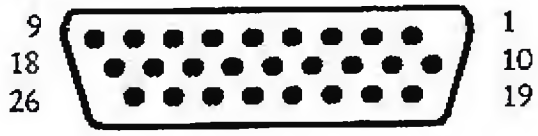
2.3.11.1 DSP Pin and Signal List

Pin	Signal	Type	Description
53,54,57, 58,60,61, 65,67,68, 70,71,75, 76,77,79, 80	A0-A15	Output	16-bit Address bus.
81,82,85, 86,87,88, 92,93,94, 96,97,99, 102,104, 105,106, 108,109, 113,114, 115,118, 119,120	D0-D23	I/O	24-bit data bus.
52	PS-	Output	Program Memory Select is driven when external program memory is referenced. This pin is not connected in the FALCON030 system.
49	DS-	Output	Data Memory Select is driven when external memory is referenced.
48	X/(Y)-	Output	This signal is used to select which external memory space is referenced by the DS- signal. This pin is not connected in the FALCON030 system.
47	RD-	Output	Read Enable is asserted to read the external memory on the data bus (D0-D23).
46	WR-	Output	Write Enable is asserted to write the external memory on the data bus (D0-D23).

Pin	Signal	Type	Description
45	BR-	Input	Bus Request allows another device to become master of the external address and data buses (D0-D23, A0-A15). This pin is tied high in the FALCON030 system.
43	BG-	Output	This signal is used to acknowledge an external bus request. It is tied high in the FALCON030 system.
123	MODA/ IRQA-	Input	Mode Select A is a dual function pin used to select the initial operating mode of the DSP56001 and to receive interrupts from and external source. This pin is tied high in the FALCON030 system selecting Mode A.
121	MODB/IRQ B-	Input	Mode Select B is a dual function pin used to select the initial operating mode of the DSP56001 and to receive interrupts from and external source. This pin is tied to reset in the FALCON030 system.
124	RESET-	Input	Reset is used to reset the DSP56001.
25,22,20, 19,16,15, 14,11	HD0-7	I/O	The Host Data Bus is used to transfer data between the host system and the DSP56001.
5,2,1	HA0-2	Input	The Host Address Bits are used to select the Host Interface Registers.
9	HR/(W)-	Input	This signal selects the direction of Host processor access.
8	HEN-	Input	This signal is used to enable the transfer of data on the host data bus.
10	HREQ-	Output	This signal is used to request service from the host processor.
6	HACK-	Input	This signal is used to receive acknowledge of a request made for DMA transfers or for interrupt acknowledge from the host processor.
27	RXD	Input	Not Connected in the FALCON030 system.
28	TXD	Output	Not connected in the FALCON030 system.
29	SCLK	I/O	Not connected in the FALCON030 system.
31,40,37	SC0-2	I/O	These pins are used for control by the Synchronous Serial Interface.
32	SCK	I/O	Serial bit rate clock for the Synchronous Serial Interface.
42	SRD	Input	Data is input into the SSI Receive Shift Register on this pin.

Pin	Signal	Type	Description
39	STD	Output	Data is transmitted from the SSI Transmit Shift Register on this pin.
	Vcc	Input	Power supply for DSP56001.
	GND	Input	Ground for DSP56001.
127	EXTAL	Input	External 32 MHz clock input.

2.3.11.2 DSP Connector Pin List

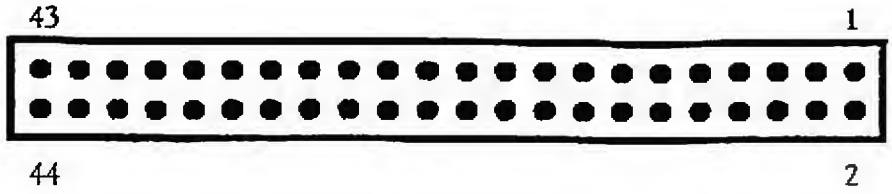


Pin	Function	Pin	Function
1	GP0	2	GP2
3	GP1	4	SDMA Play Data
5	SDMA Play Clock	6	SDMA Play Synchronization
7	No Connect	8	+12V
9	+12V	10	Ground
11	SYNC Serial I/F Control 0	12	SYNC Serial I/F Control 1
13	SYNC Serial I/F Control 2	14	Ground
15	Synchronous Serial Data In	16	Ground
17	+12V	18	Ground
19	SDMA Record Data	20	SDMA Record Clock
21	SDMA Record Synchronization	22	DSP Interrupt
23	SYNC Serial I/F Data Out	24	SYNC Serial I/F Clock
25	Ground	26	External Clock (GENLOCK)

2.3.12 IDE Interface

The FALCON030 is equipped with an IDE interface. IDE drives can be connected through an internal 44-pin connector. Chip selects and direction control for the IDE interface are provided by the COMBEL IC. The interface resides across the data bus using data bits 0-16. Four address bits are used to control the IDE interface (A2-A4).

2.3.12.1 IDE Connector Pin List



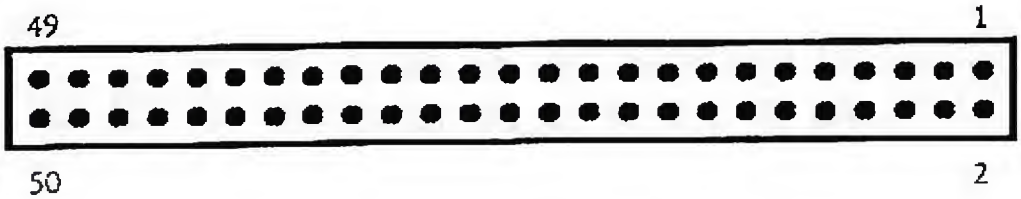
Pin	Function	Pin	Function
1	RESET	2	Ground
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DADA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	Ground	20	KEY
21	N/C	22	Ground
23	IOW	24	Ground
25	IOR	26	Ground
27	N/C	28	N/C
29	N/C	30	Ground
31	IRD	32	N/C
33	ADDR 3	34	N/C
35	ADDR 2	36	ADDR 4
37	CS0	38	CS1
39	ACT	40	Ground
41	VCC	42	VCC
43	Ground	44	N/C

2.3.13 Expansion Connector

The FALCON030 contains an expansion port connector for use with expansion boards designed for the system. The expansion port is made up of one 50-pin connector and one 30-pin connector. The connectors interface to the system through the data and address bus. External interrupts numbers 1 and 3 are provided to the connector. External bus masters can also be plugged into the expansion connector, and signals are provided for bus control and synchronization.

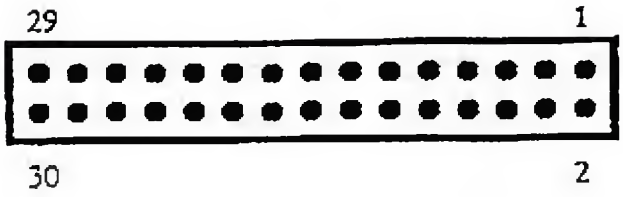
2.3.13.1 Expansion Connector Pin List

50-pin Connector J19



Pin	Function	Pin	Function
1	Ground	2	Ground
3	Bus Grant Acknowledge	4	Address Strobe
5	Lower Data Strobe	6	Upper Data Strobe
7	Read/Write	8	Data Transmit Ack
9	Function Code 2	10	Function Code 1
11	Function Code 0	12	BMODE
13	No Connect	14	Interrupt Ack
15	Combel Bus Grant Acknowledge	16	Bus Request
17	Reset	18	Halt
19	Bus Error	20	IPL0
21	IPL1	22	IPL2
23	Clock	24	Vcc
25	Vcc	26	Address 23
27	Address 22	28	Address 21
29	Address 20	30	Address 19
31	Address 18	32	Address 17
33	Address 16	34	Address 15
35	Address 14	36	Address 13
37	Address 12	38	Address 11
39	Address 10	40	Address 9
41	Address 8	42	Address 7
43	Address 6	44	Address 5
45	Address 4	46	Address 3
47	Address 2	48	Address 1
49	Expand	50	No Connect

30-pin Connector J20



Pin	Function	Pin	Function
1	Data 14	2	Data 13
3	Data 12	4	Data 11
5	Data 10	6	Data 9
7	Data 8	8	Data 7
9	Data 6	10	Data 5
11	Data 4	12	Data 3
13	Data 2	14	Data 1
15	Data 0	16	Data 15
17	Ground	18	Ground
19	Ground	20	Expansion Bus Grant
21	Interrupt 1	22	External CPU Bus Grant
23	500 kHz Clock	24	No Connect
25	MFP Interrupt Enable In	26	MFP Interrupt
27	Interrupt 3	28	Vcc
29	Vcc	30	Vcc

2.4 SYSTEM STARTUP

After a RESET (power-up or reset button) the 68030 will start executing at the address pointed to by locations 4-7, which is ROM (the MCU within the COMBO IC maps the first 8 bytes of ROM at E00000 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM. The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse). (RESET.)
2. Read the longword at cartridge address FA0000. If the data read is a magic number, execute from the cartridge (cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations are valid). If not, initialize the memory controller.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if successful.
12. If no boot disk, load the desktop ROM on board ROM.

2.5 SYSTEM ERRORS

The 68030 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen. The number of bombs equals the number of exceptions which occurred.

System errors may or may not be recoverable. Errors in loading files from disk may cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

2.5.1 Number of Bombs and Meaning

2: BUS ERROR. COMBO IC asserted bus error.

3: ADDRESS ERROR. Processor attempted to access word or long word sized data on an odd address.

4: ILLEGAL INSTRUCTION. Processor fetched an instruction from ROM or RAM which was not a legal instruction.

5: ZERO DIVIDE. Processor was asked to perform a division by zero.

6: CHK INSTRUCTION. This is a legal instruction, if software uses this, it must install a handler.

7: TRAPV INSTRUCTION. See Chk instruction.

8: PRIVILEGE VIOLATION. CPU was in user mode, tried to execute a 68030 instruction that can only be performed in supervisor mode.

9: TRACE. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.

10: LINE 1010 EMULATOR. CPU read an instruction which has '1010' as its most significant nibble. Used by TOS for low level graphics software routines.

11: LINE 1111 EMULATOR. CPU read an instruction which has '1111' as its most significant nibble.

12: Unassigned, should be no occurrence.

13: Coprocessor Protocol Violation. A read of the coprocessor has resulted in an illegal value.

14: Format Error. The format word passed to the coprocessor was invalid.

15: Uninitialized Interrupt. An interrupt was received that had not been reset.

16-23: Unassigned, should be no occurance.

24: SPURIOUS INTERRUPT. Bus error during interrupt processing.

25-31: AUTOVECTOR INTERRUPT. Numbers 4 and 2 are used, others should have no occurrence.

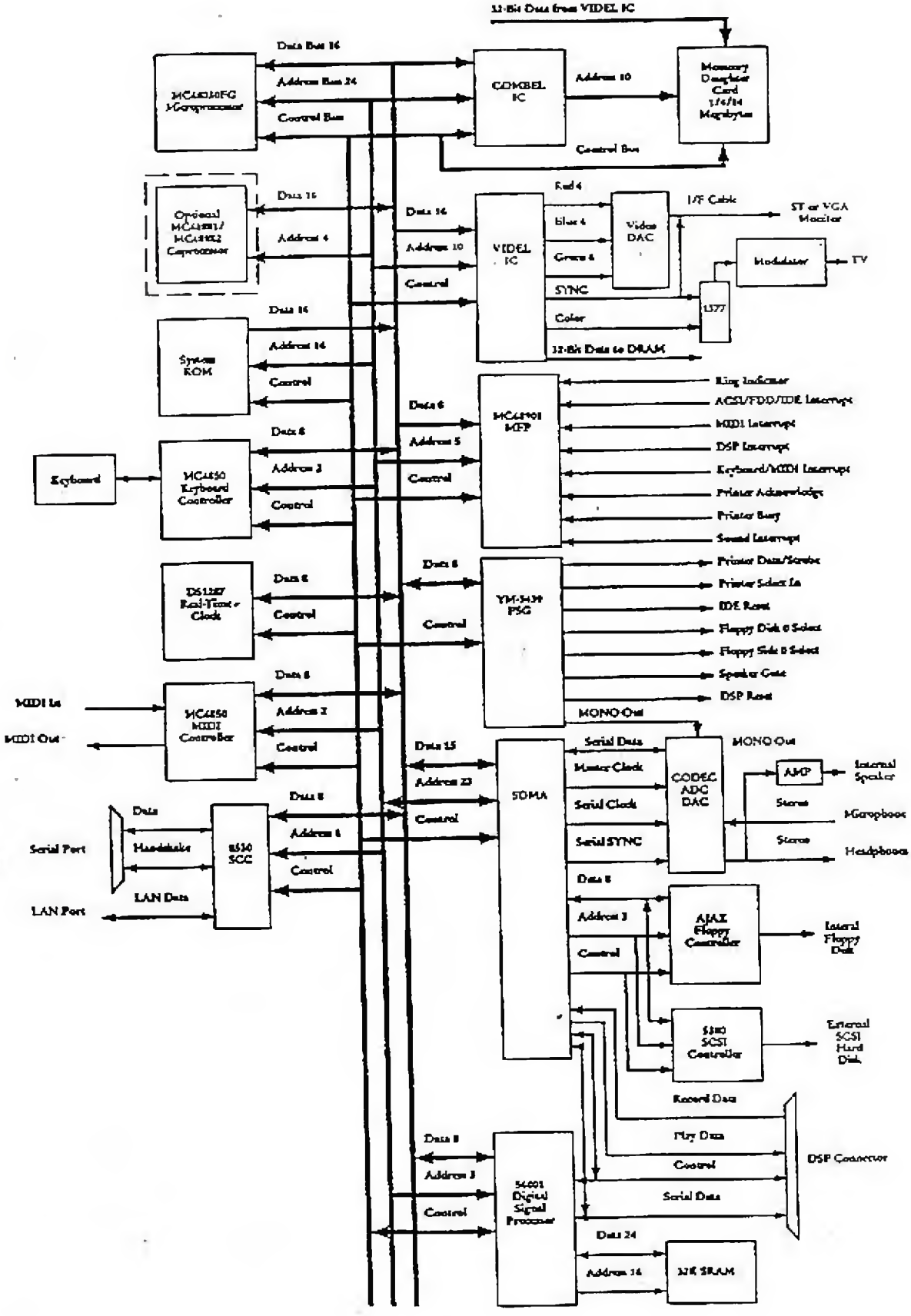
32-63: TRAP INSTRUCTION. CPU read instruction which is used to generate a software exception (such as the entry to GEMDOS, VDI, or AES).

64-79: MFP interrupts.

80-127: Reserved for Atari use.

128-255: Unused.

2.6 Overall Block Diagram



GLOSSARY

AJAX IC	Floppy Disk Controller.
6850	Also ACIA (Asynchronous Communication Interface Adapter). Each one provides an asynchronous communications channel. In the FALCON030, there are two 6850s, one for keyboard communication, and one for MIDI communication.
68901	See MFP.
BUS ERROR	COMBEL IC has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller in the COMBEL IC fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.
CPU	The 68030 microprocessor.
DMA	Direct Memory Access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, and takes place independent of the CPU, so that the CPU can be processing while DMA is taking place. The COMBEL IC arbitrates the bus between the CPU and DMA.
DMA CONTROLLER	Atari proprietary SDMA chip which controls the DMA process. All disk I/O goes through this device.
EXCEPTION	A state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also System Errors, or a 68030 reference for more detail.
COMBEL	Atari proprietary chip which ties together all system timing and control signals. It provides ROM/RAM/IO address decode, Register decode (only for registers that remain in the COMBEL), Interrupt priority encoding and IACK logic, Paddle circuit, Joystick circuit, Clock dividers, Video registers (with modifications to support up to 14MB DRAM memory space), and the Blitter.

RS232C	Electrical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the FALCON030 computers, consists of the MFP, PSG, 1488, and 1489 chips.
SUPERVISOR MODE	State of the CPU in which it is allowed to access all hardware and RAM locations, and perform some privileged instructions. Determined by the state of a bit in the Status Register.
USER MODE	State of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.
VSYNC	Signal used for vertical synchronization of CRT display device.
YM2149	See PSG.

MEMORY CONNECTOR
J17
74LS244
U43
HALF MOONS
DATA[15:0]
CPUCLK

MEMORY CONNECTOR
MEMORY CONNECTOR
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
DRAM 1MX4
U1
U2
U3
U4
U5
U6
U7
U8
J1
J2
J3
J4
MCS4150
MCS4151
MCS4152
MCS4153
MCS4154
MCS4155
MCS4156
MCS4157
USE 1MX4 DRAMS FOR 4M BYTE MEMORY, 32 BIT WIDE
FOR SIZE (16 BIT WIDE) MEMORY
MEMORY US.U6.U7.U8, USE 256K-4 DRAMS
USE 256K-4 DRAMS FOR 2M BYTE MEMORY, 32 BIT WIDE
(Default is 4M byte, 32 bit wide)